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| 10/597,822 | 08/09/2006 | Martin J. Edwards | 14509-0131US1 / P080487SE | 6742 |

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FISH & RICHARDSON PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

| EXAMINER | |
|---|---|
| MA, CALVIN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2629 | |

| NOTIFICATION DATE | DELIVERY MODE |
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| 12/08/2009 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/597,822 | EDWARDS, MARTIN J. | |
| | Examiner | Art Unit | |
| | CALVIN C. MA | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. The proposed reply filed on 09/8/2009 has been entered and entered by the examiner.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9, 11-19, and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edward et al. (US Pub: 2002/0054005) in view of Credelle et al. (US Pub 2004/0246280).

As to claim 1, Edward teaches an active matrix display (i.e. the TFT LCD) device comprising a row and column array of picture elements (see Fig. 1),

sets of row and column address conductors for selecting rows of picture elements and providing data signals to the picture elements of a selected row respectively (i.e. the column and row electrode that lead to the individual LC pixel) (see Fig. 1),

drive means for supplying selection signals and multi-bit digital data signals respectively to the set of row address conductors and the set of column address conductors (see Fig. 1, elements 21, 23, and 25), and

in which the multi-bit digital data signals supplied to the column address conductors are converted into analogue voltage levels for use by the picture elements by a plurality of serial charge redistribution digital to analogue conversion means (see Fig. 3, [0023-0024]),

each conversion means comprising at least first and second capacitances interconnectable by at least one conversion switch and between which charge is shared (see Fig. 3), and

in which the first and second capacitances of a conversion means are provided by the capacitances of two column address conductors (see Fig. 7, 19a, 19b),

However, Edward is silent the drive means is arranged to alternate the supply of data signals to the first and second column address conductors.

Credelle teaches to alternate the supply of data signals to the first and second column address conductor (i.e. Credelle teaches the alternating data line input to the LCD active matrix by creating a positive and negative pattern by which the column is driven ) (see Fig. 4, Col. 3, Lines 7-35).

Therefore it would have been obvious for one of ordinary skill in the art at the time the invention was made to have used the alternating data line design of Credelle in the Edward's LCD system (i.e. having the dual or multiple column controlling switch C 31 to have the ability to allow the circuits to alternate polarity data to the circuitry) in order to minimize the degradation in the overall display system (see Credelle [0017]).

As to claim 12 and 17, see claim 1 above, claim 12 and 17 are analyzed by the examiner as having broader scope as claim 1 and are rejected on the same ground.

As to claim 2, Edward teaches a device according to Claim 1, wherein the column address conductor of a conversion means to which the data signals are applied is changed after one or more complete multi-bit signal conversions performed by the conversion means (see [0028]).

As to claim 3, Edward teaches a device according to Claim 1, wherein the supply of data signals to the column address conductors of each conversion means is controlled by a switch arrangement (i.e. the switch a and b controls the supply to each column conductor) (see Fig. 7).

As to claim 4, Edward teaches a device according to Claim 3, wherein the switch arrangements of all conversion means are operable together by the drive means (i.e. the switch arrangement for the conversion means all work together to drive the display) (see [0021]).

As to claim 5, Edward teaches a device according to Claim 3, wherein the switch arrangement comprises a respective switch device connected between a column address conductor and a serial digital data signal output of the drive means (i.e. the switch a and b are between a column address conductor and a serial digital data signal

output).

As to claims 6 and 15, Edward and Credelle teaches a device, wherein the polarity of the voltage provided to the picture elements is inverted periodically (i.e. the polarity is inverted on the different columns by the arrangement of separate data driving circuitry) (see Kimura Fig. 4), and wherein the alternation of the column conductors of a conversion means to which a data signal is applied to generate the analogue voltage level for a given picture element is synchronized with the inversion of the picture element voltage (i.e. when combined together to inverting polarity dual driving will require a synchronized conversion process to generate the analogue voltage from the digital input data) (see Fig. 2 of Credelle and Fig. 7 of Edward).

As to claims 7 and 19, Edward and Credelle teaches a device, wherein the drive means and the conversion means are operable such that for a given picture element the column address conductor of its associated conversion means to which a data signal is applied is changed each time the polarity of the picture element voltage is inverted (i.e. the sequential driving of the TFT circuitry of Credelle clearly shows the inverting nature of the LCD driving structures) (see Credelle Fig. 2).

As to claims 9 and 16, Edward teaches a device, wherein the picture elements comprise liquid crystal display elements (see Col. 2, Lines 10-20).

As to claims 11 and 13, Edward and Credelle teaches the device in which during one mode of operation of the display device, when data signals are supplied from the drive means to the first column address conductor, the data signals are not supplied to the second column address conductor, and when data signals are supplied from the drive means to the second column address conductor, the data signals are not supplied to the first column address conductor (i.e. the double data driving alternating circuitry design ensures that the two data signal applied are not redundantly applied) (see Credelle Fig. 2).

As to claim 14, Edward and Credelle teaches the device of claim 12 in which during a first period, the controller controls the switches to cause a first multi-bit digital data signal to be sent from the column driver to a first column conductor of each pair of column conductors, and causes redistribution of charges between the two column conductors of each pair of column conductors to convert the first multi-bit digital data signal to a first analog signal, and during a second period of time, the controller controls the switches to cause a second multi-bit digital data signal to be sent from the column driver to a second column conductor of each pair of column conductors, and causes redistribution of charges between the two column conductors of each pair of column conductors to convert the second multi-bit digital data signal to a second analog signal (i.e. in the Edward's system the first and second column are charged by the capacitor at different time, this combined with the polarity inverse technique of Kimura with the dual drive system would mean that the first and second period of time of the conversion

would be applied to the different columns driven by the different sub-driver) (see Edward Fig. 3, and Credelle Fig. 2).

As to claim 18, see claim 6 above, claim 18 is analyzed to be of the same scope as claim 6 and is rejected for the same reason.

As to claims 21, 23, and 26, Edward and Credelle teaches the device in which the drive means comprises a digital data output that is arranged to alternate the supply of data signals to the first and second column address conductors of each conversion means (i.e. the alternating polarity of the supplied digital signal resulting in the inverted output of the columns as realized in the dual column control matrix structure of Edward) (see Credelle Fig. 2, Edward Fig. 3).

As to claim 22, 24, and 26, Edward and Credelle teaches the device of claim 1 in which the drive means is arranged to alternate in time the supply of data signals to the first and second column address conductors (i.e. the alternating polarity of the supplied digital signal of Credelle means that the positive and negative signal and alternate in time to create a palpable inversion effect to reduce degradation, as realized in the dual column control matrix structure of Edward) (see Credelle Fig. 2, Edward Fig. 3).

4. Claims 8, 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edward in view of Credelle et al. as applied to claim 1-7, 9 and 11-19 above, and further in view of Janssen et al. (US Patent: 6469687).

As to claims 8 and 20, Edward and Credelle teaches a device, wherein the drive means and the conversion means are operable such that for a given picture element the column address conductor of its associated conversion means.

However Edward and Credelle does not explicitly teach means to which a data signal is applied is changed every second time the polarity of the picture element is inverted. Janssen teaches the data signal that is applied is changed every second time the polarity of the picture elements is inverted (see Janssen Col. 2, Lines 4-7).

Therefore it would have been obvious for one of ordinary skill in the art at the time the invention was made to have modified the system of Edward and Credelle with the method of Janssen whereby the data signal that is applied is changed every second time the polarity of the picture element is inverted, thus reducing or eliminating sampling errors (see Janssen Col. 2, Lines 4-7).

As to claim 10, Janssen teaches a device according to Claim 9, wherein the drive means is arranged to alternate the supply of data to the first and second column address conductors with a period which is shorter than the response time of the liquid crystal material (see Col. 6, Lines 10-23).

***Response to Arguments***

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALVIN C. MA whose telephone number is (571)270-1713. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on 571-272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma
November 23, 2009

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629